PURDUE SCHOOL OF MECHANICAL ENGINEERING

ME597: FUNDAMENTALS OF MICROSYSTEMS PACKAGING

Dr. Jaesik Lee, Vice President SK Hynix USA

Seminar: Tuesday, March 24- 3:00 P.M. Mechanical Engineering ME 1012

https://purdue-edu.zoom.us/j/91592059777?pwd=nmm5W8lYIr6jlbq7OyEDPuhr4mPohZ.1

Invited Industry Talk: The Role of Semiconductor Packaging in the AI Era

Jaesik Lee is a Vice President at SK Hynix USA, where he is leading a team for future advanced packaging technology development and pathfinding in system level perspectives including SOC and HBM. His current interests include 2.5D and 3D advanced packaging technology and High bandwidth memory (HBM) packaging. Prior to joining SK Hynix, he had been with Meta, Google, Nvidia, and Qualcomm, working on 2.5D packaging technologies developments and manufacturing for High Performance Computing (HPC) and AR devices. Jaesik received his PhD degree in mechanical engineering at University of Waterloo, Waterloo, Canada.

Description of Presentation: The rapid advancement and proliferation of Generative Artificial Intelligence (GenAi) and large language models (LLMs) have significantly dominated the technological landscape, escalating the computing power requirement along with enhanced computing efficiency. Heterogeneous integrations with Logic, Memory, and chiplets on a single interposer has become a mainstream solution to address the computing power requirement by increasing bandwidth, latency, and power consumption. In memory perspective, High Bandwidth Memory (HBM) has been a critical building block to meet the system requirements since SK Hynix introduced HBM1 in 2013. In this presentation, I will introduce SK Hynix's plans in West Lafayette and then discuss advanced packaging technologies used in the accelerators followed by the HBM stacking innovations and their challenges associated with advance packaging technologies.

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