



Dr. Tiwei Wei

**Postdoctoral Research Scholar
Stanford University**

Thursday, February 3rd

9:00 AM—WALC 2087

Zoom Link: <https://bit.ly/H3D-ACT>

Passcode: 921489

Heterogeneous 3D Integration and Advanced Cooling Technologies

Abstract:

Advanced semiconductor packaging is playing a crucial role to drive system performance and functionality. With the increasing demand for emerging and growing computing needs, heterogeneous three-dimensional (3D) integration with fine-pitch, high-density interconnections, and multi-chip stacks are very promising in the future. The aggressive interconnects pitch scaling and nanoscale via interconnections make the process development and reliability more and more challenging. On the other hand, this high-density 3D integration system has resulted in a substantial increase in both heat flux and power density (W/cm^3). High-performance, energy-efficient thermal management solutions are needed to tackle this thermal challenge. During this talk, I will first present the copper 3D interconnects manufacturing technologies and their applications in different heterogeneous 3D integration systems. The second part of this talk will focus on the modeling and package integration of advanced thermal cooling solutions, including impingement jet cooling, manifold-based embedded microchannel cooling and cryogenic cooling.

Biography:

Tiwei Wei is currently a postdoctoral research scholar in the NanoHeat lab at Stanford University. He received his Ph.D. degree in the 3D system integration department at Interuniversity Microelectronics Centre (imec) and KU Leuven, Belgium in 2020. He joined imec in 2015, starting the Ph.D. research with developing electronic cooling solutions for high-performance 3D systems. Before joining in imec, he worked as a researcher staff in Tsinghua University and Hong Kong University of Science and Technology, from 2011 until 2015, where he worked on advanced microelectronic packaging techniques. His current research interests include impingement jet cooling and embedded microchannel cooling for heterogeneous 3D integration. He serves on the session chair and technical program committee of several electronic packaging conferences, including IEEE ESTC, REPP, 3DIC and EPTC. He is currently the vice-chair of IEEE Electronic Packaging Society (EPS) Silicon Valley Chapter, with the mission to promote the education of local STEM students in the area of electronic packaging.