PURDUE UNIVERSITY | Elmore Family School of Electrical and Computer Engineering

Computer Engineering Seminar Series

Dr. Michael D. Powell (Class of '05)

Principal Engineer and Lead Product Architect
Intel

Wednesday, April 24, 2024
10:30 A.M. – 11:30 A.M.
Purdue Graduate Student Center
504 Northwestern Ave. ~ Room 105A/B

Architecting for Flexibility and Value with Future Intel® Xeon® Processors

Abstract
The future Intel® Xeon® 6 processor introduces a new architecture that provides the scalability, power efficiency, performance, and versatility necessary to address the growing needs of datacenter workloads and deployments. This talk will discuss advancements in both the IO and Memory subsystems which deliver improvements in performance and platform flexibility. The architecture's logically monolithic compute cluster delivers significantly better performance-per-watt and performance-per-thread over previous products and sets the foundation for future Intel Xeon processors, codenamed Granite Rapids and Sierra Forest.

Bio
Michael D. Powell is a Principal Engineer in Datacenter Processor Architecture at Intel and the lead product architect for the Intel® Xeon® 6 CPU, codenamed Granite Rapids. Prior to his current role, Michael developed core and SoC power models, reliability models, and resilient architectures. He championed leveraging silicon variability to improve CPU reliability and performance, leading to the development of Intel Turbo Boost Max 3.0 and a 2017 Intel Achievement Award. Michael is an inventor on 8 US patents with others pending, and he is an author on over a dozen publications.

Michael joined Intel Massachusetts in 2005 after completing his BS in Electrical Engineering and Ph.D. in Electrical and Computer Engineering at Purdue University. During his graduate program, Michael was awarded a National Science Foundation Graduate Research Fellowship and an Intel PhD Fellowship.

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