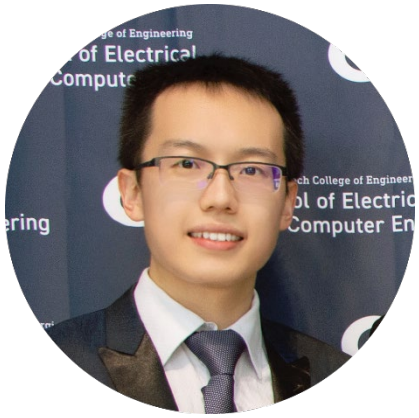
AI Hardware Faculty Candidate Seminar



Zishen Wan
PhD Candidate
Georgia Institute of Technology

Monday, March 9th
10:30 A.M • POTR 234

Architecture Physical Intelligence: Cross-Stack Co-Design from Systems to Silicon

Abstract
Physical intelligence – where embodied agents perceive, reason, plan, and act in the physical world – is emerging as a new computing frontier spanning robotics, autonomous systems, and spatial AI. However, today's physical intelligence systems remain constrained by high latency, energy cost, and fragile reliability, due to fundamental mismatch between their compositional nature and existing computing architectures. The core challenge extends beyond algorithms, to how we architect computing systems and silicon that natively support intelligence that reasons and adapts under real-world constraints.

In this talk, I will present a principled cross-stack system-architecture-silicon co-design approach to building the computational foundations for physical intelligence. I will first introduce REASON, a flexible hardware architecture culminating the first programmable SoC tapeout for efficient neuro-symbolic cognition. REASON integrates unified kernel abstractions, flexible dataflows, memory-centric computing, end-to-end compilation flow, and adaptive power management, enabling efficient cognition in silicon. Building on this foundation, I will present ReCA, an integrated hardware architecture that bridges high-level cognition and low-level autonomy under stringent power and latency constraints by leveraging spatial-aware runtimes, memory layout optimizations, and heterogeneous fabrics. Finally, I will highlight our agile SoC design flows that translate evolving physical intelligence workloads into efficient silicon implementations.

By bridging computer architecture, system software, and silicon validation, my research establishes adaptive, accelerator-rich computing substrates for physical intelligence. This work advances a vision in which AI and hardware are co-designed, co-reason, and co-adapt, architecting future computing systems as active enablers of intelligence in the physical world.

Bio
Zishen Wan is a postdoctoral fellow at Harvard University, working with Prof. Vijay Janapa Reddi. He received his Ph.D. from Georgia Tech, advised by Profs. Arijit Raychowdhury and Tushar Krishna. His research focuses on computer architecture, with an emphasis on cross-stack co-design of systems, architectures, and silicon for physical intelligence. His work appears in venues including ASPLOS, MICRO, HPCA, JSSC, ISSCC, and DAC, and has been recognized with Best Paper Awards at DAC, CAL, and SRC JUMP2.0, First Place Awards in DAC PhD Forum and ACM Student Research Competition, and honorable mention in IEEE Micro Top Picks. He is a recipient of Qualcomm, Baidu, and CRNCH PhD Fellowships, and was named as ML and Systems Rising Star and Cyber-Physical Systems Rising Star. His research has been featured in MIT Technology Review and Fortune, and adopted by industry partners including Intel, IBM, and Google. For more information, please visit https://zishenwan.github.io/.

Host
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