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From Energy-Efficient Digital SoCs to Adaptive Neuromodulation: Opportunities in Co-Design and Run-time Optimization

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Abstract

For over half a century, improvements in semiconductor technology have advanced performance and energy-efficiency of integrated circuits and systems. During this time, the approach to hardware design – a careful, often creative, but highly focused effort – has remained largely changed. However, diminishing benefits offered by each new process node have placed a renewed onus on design, and underscoring the shortcomings of this traditional approach. In this talk, I highlight two critical design approaches – co-design and run-time computational techniques – that are poised to play an increasingly important role in building future systems for computing, communication and sensing. Co-design leverages a more comprehensive problem perspective to realize impactful solutions at the intersection of systems, architecture, circuits and process technologies. Meanwhile, run-time system control and optimization techniques have effectively leveraged our ability to perform efficient, low-latency computation to significantly advance system capabilities.

We will first examine the impact of these approaches in the context of power management through the design of energy-efficient and domain-scalable Single Inductor Multiple Output (SIMO) regulators. I will provide an overview of SIMO regulation and describe a critical but largely unaddressed drawback of SIMO regulators. Left unaddressed, this drawback invalidates this promising technology from practical realization. I discuss two solutions, enabled by co-design and runtime-computation respectively, that we have proposed to address this problem. The effectiveness of these approaches is evaluated through measurement results on a dual-processor 4-domain SIMO-regulated SoC in 65nm CMOS. Finally, I provide an overview the broader potential of these design principles to address other important research problems.

Bio

Visvesh S. Sathe received the B.Tech. degree from the Indian Institute of Technology, Bombay and the M.S. and Ph.D. degrees from the University of Michigan, Ann Arbor. He is currently an Associate Professor of Electrical and Computer Engineering at the University of Washington where he leads the Processing Systems Lab (PSyLab), focused on research associated with energy-efficient computing and implantable electronics. Prior to joining the University of Washington, he served as a Member of Technical Staff in the Low-Power Advanced Development Group at AMD, where his research focused on inventing and implementing circuit, clocking and supply mitigation technologies in next-generation microprocessors. These technologies include high-speed digital circuits, adaptive clocking for supply noise mitigation and resonant clocking. His current research interests include implementation of run-time hardware control and optimization in digital and mixed-signal systems over a range of applications. He is the recipient of an NSF Career award in 2019 and more recently, the Intel outstanding researcher award in 2021. He serves on the technical program committee of the IEEE Custom Integrated Circuits Conference, and as a distinguished lecturer of the Solid-State Circuits Society.

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