PURDUE UNIVERSITY | Elmore Family School of Electrical and Computer Engineering

Lecturer Candidate

Dr. Junfei Li

University of Texas, Rio Grande Valley

Friday, March 4, 2022
9:30 A.M. – 10:30 A.M.
BHEE 317
https://purdue-edu.zoom.us/j/99411911352

Introduction to Sequential Logic Design

Abstract: This teaching presentation designed to introduce sequential circuits to students who have only designed combinational logic circuits. The goals are 1) to set up the new techniques for state machine analysis and design through a template state machine structure and by focusing on state transitions and 2) to describe how the most important memory element - a D flip-flop works. Through examples, students will be learning how to identify key elements of a state machine and be practicing state machine analysis and design tools such as state diagram, state transition table, timing diagram, and Verilog HDL.

Bio: Dr. Junfei Li has been with the University of Texas Rio Grande Valley and its legacy institution since he graduated from the University of Texas at Austin with a Ph.D. degree in Electrical and Computer Engineering in 2002. He has a background and experience in radar and electromagnetics. Recently he has been teaching digital design and a junior level lab course. In response to the remote lab teaching needs during the covid-19 pandemic, he developed an online platform featuring design entries using schematic diagrams, breadboard layouts, HDL source codes, and embedded programming in C/C++ and python along with over 40 FPGA boards for real-time hardware testing on the web. The platform from ECE Labs has been successfully used by hundreds of college students, summer camps, and three recent Xilinx University Program workshops.