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Devices & ASICs for Machine Intelligence, IoT, and Post-Quantum Cryptography

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Abstract

The high demand for AI services in conjunction with a dramatic chip shortage along with technology leaps such as 5/6G networks, cybersecurity threats, and quantum algorithms have resurrected a R&D push for advanced devices, computing capability, and machine intelligence. To address such demands and to explore novel device/circuit/system technologies unique opportunities exist, for example, given by emerging materials, highly functional devices, and algorithm-hardware synergies to pioneer next-generation sensors, processors, and accelerators. In this seminar I will share my latest insights on fundamental complexity scaling and algorithm-hardware homomorphism on the one hand, and device- circuit- and system-level demonstrations on the other. In the first part, I will introduce advances in electronic and optoelectronic devices including quantum matter. Starting from earlier work at Intel on next-generation FETs and molecular-based tunnel-junction memory devices, I share recent demonstrations of a 56Gbps ITO-based electro-optic modulator being 1,000x more compact than Silicon PDK solutions. Utilizing our one-of-a-kind 2D material printer system, I will introduce the concept of strainoptronics enabling high gain-bandwidth-product photodetectors and a 60GHz-fast Graphene modulator. I will conclude the device portion with highlighting recent realizations of laser sources including a high-speed coupled-cavity VCSEL.

Electronic-photonic ASIC compute paradigms hold promise to enable non-iterative O(1) runtime complexity, ps-short latency, and TOPS/W throughputs. This opens prospects for next-generation hardware both for AI cloud services but also for accelerating edge computing such as enabled by compact and efficient PIC-CMOS co-designs pushing the SWAP envelope. In the second part, I will introduce a novel memristive RAM enabling zero-static power consumption suitable for AI edge applications and highlight our photonic tensor core ASIC accelerator leveraging multi-channel parallelism. Beyond matrix-matrix multiplication acceleration, I will show our Convolution Theorem-based accelerator enabling 1000x1000 matrix-size convolutions at 100us latency, or about 10x faster than today's GPUs, along with a cutting-edge CNN chip implementation. Finally, having solved the complex-signal convolution I will show a Montgomery Multiplier for a data-center RSA public-key cryptosystem, and close by highlighting our contributions in post-quantum secure-hash-algorithm (SHA) ASICs towards accelerating blockchain operations. I will conclude with an R&D outlook for the next decade and share examples of my passion supporting values and educational activities on diversity & inclusion.

Bio

Volker J. Sorger is an Associate Professor in the Department of Electrical and Computer Engineering and the Director of the Institute on AI & Photonics, the Head of the Devices & Intelligent Systems Laboratory at the George Washington University. His research areas include devices & optoelectronics, AI/ML accelerators, mixed-signal ASICs, quantum matter & processors, and cryptography. For his work, Dr. Sorger received multiple awards including the Presidential PECASE Award, the AFOSR YIP Award, the Emil Wolf Prize, and the National Academy of Sciences award of the year. Dr. Sorger is an Associate editor for OPTICA, serves on the board of Chip, and was the former editor-in-chief of Nanophotonics. He is a Fellow of Optica (former OSA), a Fellow of SPIE, a Fellow of the German National Academic Foundation, and a Senior Member of IEEE. He is a co-founder of Optelligence Company.

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