

Physics of Nanoscale Transistors: An Introduction to Electronics from the Bottom Up

Mark Lundstrom

**Tuesday, August 5, 2008; 1:30-2:30pm
Burton Morgan Bldg., Room 121**

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ABSTRACT

Transistor scaling has pushed channel lengths to the nanometer regime, and advances in nanoscience are opening up many new possibilities for devices. To realize these opportunities, our traditional understanding of electronic devices needs to be complemented with a new perspective that begins from the nanoscale. My objectives in this talk are: 1) to describe a way of understanding MOSFETs that is much more suitable than traditional approaches when the channel lengths are of nanoscale dimensions, and 2) to introduce the “bottom up” approach, a way of understanding nanoscale electronics very generally. This talk will provide a starting point for those interested in exploring the electronics from the bottom up approach through the resources of nanoHUB.org.

For more information, see:

<http://www.nanohub.org/resources/5067>

WHEN

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WHERE

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Prof. Lundstrom earned bachelor's and master's degrees in electrical engineering from the Univ. of Minnesota in 1973 and 1974, respectively. He joined the Purdue faculty upon completing his doctorate on the West Lafayette campus in 1980. He is currently the Don and Carol Scifres Distinguished Professor of Electrical and Computer Engineering and Founding Director of NSF Network for Computational Nanotechnology.

Lundstrom's current research interests center on the physics and limits of small electronic devices, especially nanoscale transistors, on carrier transport in semiconductor devices and on numerical methods for device simulation.



The Network for Computational Nanotechnology is supported by the National Science Foundation, Indiana 21st Century Fund, and ARO. It has a vision to pioneer the development of nanotechnology from science to manufacturing through innovative theory, exploratory simulation, and novel cyberinfrastructure.