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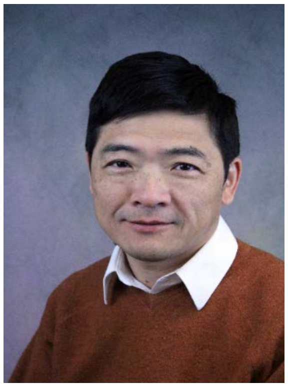
Birck Nanotechnology Center



Dr. Peide Ye is Richard J. and Mary Jo Schwartz Professor of Electrical and Computer Engineering at Purdue University in USA. He received Ph.D. from Max-Planck-Institute of Solid State Research, Stuttgart, Germany, in 1996. Before joining Purdue faculty in 2005, he worked for NTT, NHMFL/Princeton University, and Bell Labs/Lucent Technologies/Agere Systems. His current research is focused on ALD high-k integration on novel channel materials including III-V, Ge, complex oxides, graphene and other 2D crystals. He authored and co-authored more than 220 peer reviewed articles and 400 conference presentations. He is a Fellow of IEEE and APS (American Physical Society).

Birck Faculty Seminar
Professor Peide Ye

Thursday, February 1, 2018
12:00pm – 1:00pm
BRK 2001 – Lunch Provided

The so-called Boltzmann Tyranny defines the fundamental thermionic limit of the subthreshold slope (SS) of a metal-oxide-semiconductor field-effect transistor (MOSFET) at 60 mV/dec at room temperature and, therefore, precludes the lowering of the supply voltage and the overall power consumption. Adding a ferroelectric negative capacitor to the gate stack of a MOSFET may offer a promising solution to bypassing this fundamental barrier. [1] Meanwhile, two-dimensional (2D) semiconductors, such as atomically thin transition metal dichalcogenides (TMDs) due to their low dielectric constant, and ease of integration in a junctionless transistor topology, offer enhanced electrostatic control of the channel. [2] We combine these two advantages and demonstrate for the first time a molybdenum disulfide (MoS_2) 2D steep slope transistor with a ferroelectric hafnium zirconium oxide layer (HZO) in the gate dielectric stack. This device exhibits excellent performance in both on- and off-states, with maximum drain current of 510 μA/μm, sub-thermionic subthreshold slope and is essentially hysteresis-free. In this talk, we will review the experimental progress at Purdue University on MoS_2 n-type 2D NC-FETs, WSe_2 p-type 2D NC-FETs, Ge CMOS NC-FETs and nano-membrane β-Ga_2O_3 NC-FETs for wide bandgap CMOS applications. [3] The work is in close collaborations with Mengwei Si, Wonil Chung, Mark Su of NDL/Taiwan, Profs. Alam and Shakouri's groups at Purdue University.

[1] S. Salahuddin and S. Datta, Nano Lett., vol. 8, pp. 405-410, 2008. [2] Chungsheng Jiang et al. IEEE JEDS 2018. [3] M. Si et al. Nature Nanotechnology vol. 13, pp. 24-28, 2017; M.Si et al. IEDM 2017; W. Chung et al. IEDM 2017; M. Si et al. ACS Omega 2017, 2, 7136-7140.

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