Devices & ASICs for Machine Intelligence and Post-Quantum Cryptography

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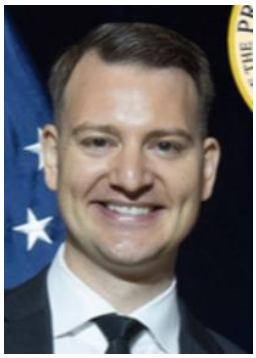

Monday, January 31st, 2022

10:00 am EST · BIRCK 1001

Seminar(10am): https://purdue-edu.zoom.us/j/93011624603

Fireside Chat (11 am): https://purdue-edu.zoom.us/j/95324226393

Event Agenda: Volker J. Sorger is an Associate Professor in the Department of Electrical and Computer Engineering and the Director of the *Devices & Intelligent Systems Laboratory* at the George Washington University. For the first hour of the event, Volker will give a 45-minute lecture covering the material presented in the abstract below followed by 15 minutes of Q&A. Then at 11 am, he and Blake Wilson will engage in a fireside chat to discuss emerging frontiers at the crossroads of machine learning, quantum computing, and optics. This event is co-hosted by the Elmore Center at Purdue University and the Quantum Science Center at Oak Ridge National Lab, both of which are exploring the emerging frontiers of innovation at the crossroads of quantum and AI.

Abstract: The high demand for AI services in conjunction with a dramatic chip shortage along with technology leaps such as 5/6G networks, cybersecurity threats, and quantum algorithms have resurrected an R&D push for advanced information processing and computing capability. To address this demand and explore novel technology roadmaps, unique opportunities exist, for example, given by algorithmic parallelism of digital-analog mixed-signal non-van Neuman accelerators. Especially electronic-photonic ASIC compute paradigms hold promise to enable non-iterative $\boldsymbol{O}(1)$ runtime complexity, ps-short latency, and TOPS/W throughputs. This opens prospects for next-generation hardware both for AI cloud services but also for accelerating edge computing such as enabled by compact and efficient PIC-CMOS co-designs pushing the SWAP envelope. As both a professor and a co-founder of a venture, in this seminar, I will share my latest insights on fundamental complexity scaling and algorithm-hardware homomorphism on the one hand, and device- circuit- and system-level realizations on the other. I will introduce a novel photonic RAM capable of zero-static power consumption suitable for AI edge applications and highlight our mixed-signal tensor core ASIC demonstration leveraging parallelism including software-stack. Beyond matrix-matrix multiplication acceleration, I will show a Convolution

Theorem-based accelerator enabling 1000x1000 matrix-size convolutions at 100us latency, or about 10x faster than today's GPUs. At the device level, I will share advanced optoelectronics and quantum matter including a 20Gbps ITO-based modulator being 1,000x more compact than Silicon and LN modulators, discuss strainoptronic detectors with high gain-bandwidth-product and a 100GHz fast VCSEL, and share a path for an electrically-driven quantum source. Finally, having solved the complex-signal convolution I will show a Montgomery Multiplier for a data-center RSA public-key cryptosystem, and conclude by highlighting our recent post-quantum secure-hash-algorithm (SHA) system accelerating blockchain operations.

Bio: Dr. Sorger is a co-founder and the President of Optelligence Company. For his work, Dr. Sorger received multiple awards among are the Presidential Early Career Award for Scientists and Engineers (PECASE), the AFOSR Young Investigator Award (YIP), the Hegarty Innovation Prize, and the National Academy of Sciences Award of the year. He is a Fellow of Optica (former OSA), a Fellow of the German National Academic Foundation, and a Senior Member of IEEE and SPIE. Dr. Sorger serves as an Associate Editor for OPTICA and was the former Editor-in-Chief of Nanophotonics. For further details visit sorger.seas.gwu.edu and op.company.