RAMESH VENUGOPAL
3600 Alma Road, Richardson TX-75080, Tel: +1 214-868-9873, Email: ramesh.venugopal@ti.com

OBJECTIVE— Seeking the position of Managing Director- Birck Nanotechnology Center.

STATUS— Permanent Resident

WORK EXPERIENCE

Team Leader in **Analog Technology Development (ATD)**, Texas Instruments (TI) Inc, Dallas **Jan 2007-present**

- Lead the Technology Computer Aided Design (**TCAD**) team for Product Development. This cross-functional team (**10 PhDs**) enables reuse of process technology across multiple customers (including Seagate, Hitachi, and Continental Tevis) with minimal process re-design ($3B Revenue)
- Lead negotiations with design/product teams (in Dallas, Japan, Germany) to set technology specifications
- Develop, and Yield process technology across multiple semiconductor fabrication units (Dallas, Japan, Germany)
- Negotiate with Design Automation software vendors ($1M budget) to customize ATD's TCAD software platforms
- Consultant to the IEEE, National Science Foundation, American Physics Society, and DARPA (Defense Research)

Member Technical Staff in Silicon Technology Development (SiTD), TI, Dallas **Jun 2003-Jan 2007**

- Lead the technology road mapping team (45nm and 32nm technologies). Customers include Nokia, Ericsson and SUN ($3B Revenue).
- Present cost-benefit analysis of emerging technologies to the CTO, and the leadership team ($400M R&D budget)
- Lead research initiatives at institutes such as LETI (France), IMEC (Belgium) , UCLA, UT-Austin, and Purdue

Summer Intern at Motorola, Austin, and at the Los Alamos National Labs, New Mexico **1999, 2000**

- 2 internships that involved developing software platforms to design/evaluate novel transistor architectures

Senior Engineer at Kinetic Honda Motors, Pune, India **May 1994-Dec 1995**

- Lead a 4 member team to manufacture connecting rods for scooter engines ($45M Revenue)
- Negotiate with tool vendors and plan the cutting tool inventory for the scooter assembly line ($0.5M budget)

EDUCATION

- **Executive MBA** University of Chicago (In Progress)
- **Ph.D.** Electrical and Computer Engineering: Purdue University (GPA 3.8/4.0) **06/2003**
  - Co-developed nanoMOS, the first open-source software to simulate nano-transistors. nanoMOS is a free software and has hundreds of users from 16 countries
- **M.S.** School of Mines and Earth Sciences: University of Utah (GPA 3.85/4.0) **05/1998**
  - Co-developed MillSoft, the first open-source software to simulate grinding mills. Millsoft is a commercial product used by more than 20 mining companies worldwide
- **B.E. First Class with Distinction** College of Engineering, Pune, India **06/1994**
  - Developed Cadmium-Telluride/Polymer Films for Solar Cell Applications

HONORS

- **Two promotions** (from specialist to expert to team lead) and **3 "Innovator of the Quarter"** awards, in 4.5 years at TI
- **TI's representative** (nominated) to the technical advisory board of the Semiconductor Research Corporation (SRC), and the Center for Computational Nanotechnology (NCN)
- Member **(nominated)** of **TI's patent review panel**
- **7 patents**, two of which are used in chips that generate more than $1B in revenue for TI
- **7 Invited Talks** and **14 articles** in peer reviewed journals, receiving **more than 450 citations** in publications such as the IBM Journal of Research, Science, and the New York and EE-times
- Member of a **Purdue panel (invited from TI)** to review the impact of globalization on the engineering curriculum
- **Intel PhD Fellowship** (2001-02) for "Innovations in Nanotechnology" (1 of 34 recipients nationwide)
- **PhD fellowship** (Purdue,1998-00) , **Teaching Award** (1997), **Graduate Scholarship** (University of Utah, 1996-98)

MISCELLANEOUS

- Coordinate TCAD training programs for 160 engineers at TI & mentoring graduate students at many universities
- Event Coordinator, and Coordinator of Asha's (non-profit) marathon program (the Strides of Hope), Amateur Historian
- Proficient in C/C++, OpenGL, Matlab, Visual Basic, and Unix/Windows-XP/Linux

APPENDIX

I INVITATIONS AND BOOK CHAPTERS

- Invited to the "Advanced Computational Software Collection (ACTS) workshop," Lawrence Berkeley National Laboratory, 2001
- Tutorial- The Green's Function Approach for MOSFETS, R. Venugopal, S. Goasguen, S. Datta and M. Lundstrom, University of Illinois at Urbana Champaign, May 2002.
- Talk- Transport in Nanoscale Devices, R. Venugopal and M. Lundstrom, Intel Corporation, July 2002.
- Talk- Simulating Electron transport in nano-transistors: Silicon and Beyond, R. Venugopal and M. Lundstrom, American Physics Society (APS) Meeting, March 2003.
- Talk- Large scale simulation of nanotransistors, R. Venugopal, S. Goasguen and M. Lundstrom, IBM, 2004.
- Contributions to "The Handbook of Theoretical and Computational Nanotechnology," American Scientific Publishers, 2005
- Talk- Design of CMOS Transistors to Maximize Circuit FOM - Logic and SRAM Challenges, R. Venugopal, S. Chakravarthi and P.R. Chidambaram, Materials Research Society, March 2007.

II PATENTS AND INVENTION DISCLOSURES

- R. Venugopal and C. Wasshuber, "A novel pitch multiplication process", 2004 (Also filed in China and Taiwan)
- R. Venugopal, C. Wasshuber and D. Scott, "An N+ poly on high-k gate stack for CMOS technology", 2005
- R. Venugopal, S. Chakravarthi and C. Bowen, "Super-halo formation using a reverse flow for halo implants to improve circuit figure of merit (FOM)", 2005 (Used in Nokia Chips)
- S. Ekbote, S. Chakravarthi and R. Venugopal, "Method of forming a semiconductor device with source/drain nitrogen implant, and related device", 2006 (Used in SUN and Nokia Chips)
- R. Venugopal and Z. Wu, "A Novel CMOS device with improved SRAM density and yield", 2007
- R. Venugopal, Z. Wu and S. Butler, "Novel CMOS device with improved performance (with metal gate on NMOS)", 2007
- R. Venugopal, Z. Wu and X. Wang, "A novel CMOS device with enhanced stress in the NMOS ", 2007

III PUBLICATIONS (citation information from the Science Citation Index & Google Scholar)

- R. Venugopal, S. Chakravarthi and P. R. Chidambaram, "Design of CMOS transistors to maximize circuit FOM using a coupled process and mixed mode simulation methodology," IEEE Electron Device Letters, 27, p. 863, 2006. **Citation Count- 20.** Also cited by the EEtimes
- R. Venugopal, S. Goasguen, S. Datta, and M. S. Lundstrom, "Quantum mechanical analysis of channel access geometry and series resistance in nanoscale transistors," Journal of Applied Physics, 95, p.292, 2004. **Citation Count- 27**
- R. Venugopal, M. Paulsson, S. Goasguen, S. Datta, and M. S. Lundstrom, "A simple quantum mechanical treatment of scattering in nanoscale transistors," Journal of Applied Physics, 93, p.5613, 2003. **Citation Count- 58**
- Z. Ren, R. Venugopal, S. Datta, and M. S. Lundstrom, "nanoMOS-2.0: A Two-dimensional Simulator for Quantum Transport in Double Gate MOSFETs," IEEE Transactions on Electron Devices, 50(9), p.1914, 2003. **Citation Count- 57.** nanoMOS (http://www.nanohub.org/resources/?id=110) is a free software product that is available on the Purdue NanoHub.
- R. Venugopal, Z. Ren, S. Datta, M. S. Lundstrom and D. Jovanovic, "Simulating Quantum Transport in Nanoscale MOSFETs: Real vs. Mode-space Approaches," Journal of Applied Physics, 92, p.3730, 2002. **Citation Count- 72**
- R. Venugopal, Z. Ren and M. S. Lundstrom, "Simulating Quantum Transport in Nanoscale MOSFETs: Hole Transport, Subband Engineering and Boundary Conditions," IEEE Transactions on Nanotechnology, 2(3), p. 135, 2003 **Citation Count- 17**
- S. Goasguen, R. Venugopal, and M. Lundstrom, "Modeling transport in nanoscale silicon and molecular devices on parallel machines," 3rd IEEE Conference on Nanotechnology, 2, p. 398, 2003 **Citation Count- 5**
- Svizhenko, M. Anantram, T. Govindan, B. Biegel and R. Venugopal "Two dimensional Quantum Mechanical Modeling of Transistors," Journal of Applied Physics, 91, p.2343, 2002. **Citation Count- 126**
- Z. Ren, R. Venugopal, S.Datta and M. S. Lundstrom "Examination of Design and Manufacturing Issues in a 10nm Double Gate MOSFET using Nonequilibrium Green's Function Simulation," International Electron Device Meeting (IEDM) Tech. Digest 2001. **Citation Count- 28**
- Z. Ren, R. Venugopal, S.Datta, M. S. Lundstrom, D. Jovanovic and J. G. Fossum "The Ballistic Nanotransistor: A simulation study," IEDM Tech. Digest 2000. **Citation Count- 42.** Also cited by the New York Times in 2001
- D. Jovanovic and R. Venugopal, "Computational techniques for the nonequilibrium quantum field theory simulation of MOSFETs," 7th International Workshop on Computational Electronics, Glasgow 2000. **Citation Count- 5.**
- R. Venugopal and R. K. Rajamani "3D Simulation of Charge Motion in Tumbling Mills by the Discrete Element Method," Powder Technology, 115(2), 2001. **Citation Count- 10.** The first 3D version of MillSoft
- R. K. Rajamani, B. K. Mishra, R. Venugopal and A. Datta "Discrete Element Analysis of Tumbling Mills," Powder Technology, 109(1), 2000. **Citation Count- 16**
- R.K. Rajamani, B.K. Mishra, P. Songfack and R. Venugopal, "Millsoft- simulation software for tumbling-mill design and trouble shooting," Mining Engineering, 51(12), 1999. MillSoft is a commercial product (www.processeng.com/index.asp?pg=millsoft)