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The MVS Nanotransistor Model: A Case Study in Compact Modeling

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Abstract: The MIT virtual source (MVS) nanotransistor model provides a simple, physical description of transistors that operate in the quasi-ballistic regime. With only a few empirical parameters that are easily obtained through device characterization, the MVS model has served well for technology benchmarking and more recently it was extended to a full-fledged compact model and validated via circuit simulation and comparison with experimental data on both silicon and III-V transistors.

In this talk, I will present my view on building an industry-standard compact model by using the MVS model as a case study. In the first part of the talk, I discuss mathematical issues, such as the smoothness of functions and their higher-order derivatives in connection with the MVS model. While mathematical smoothing techniques are commonly used in compact models to ensure convergence of circuit simulation, they may also produce undesirable and misleading artifacts in simulation. Examples from the MVS model will be used to highlight the merits and limitations of commonly used mathematical smoothing techniques. I will also introduce the definition and testing methodology for MOSFET symmetry and discuss the response of the MVS model to the various symmetry operations.

The performance of a Verilog-A model depends on being aware of and avoiding the use of performance-inhibiting constructs present in the language. In the second part of the talk, I will discuss “*language constructs to avoid*” in writing Verilog-A code by showing specific examples from the MVS Verilog-A implementation. Resolving some of the issues present in our current MVS model implementation has proven to be challenging. My goal for this talk is to start an open discussion about compact models and their implementation issues. Audience feedback is strongly encouraged.

Bio: Shaloo Rakheja received the B.Tech. degree in electrical engineering from Indian Institute of Technology, Kanpur, India, in 2005, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology in 2009 and 2012, respectively. She is currently a Postdoctoral Associate with Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge and will be joining the department of Electrical and Computer Engineering at New York University as Assistant Professor in January 2015. She has co-authored several international conference and refereed journal publications, four book chapters and contributed to the chapter on Emerging Interconnects in ITRS 2011. She received the Intel PhD Fellowship for the academic year 2011-2012 and the ECE Graduate Research Assistant Excellence Award for the academic year 2011-2012. Her research interests are in alternate state variable devices, non-Boolean and analog-like system architectures, neuromorphic or other biologically-inspired devices, energy harvesting for sensor networks and other mobile devices, and flexible and transparent electronics and optoelectronics for ubiquitous systems.