

Negative Capacitance Ferroelectric Transistors: A Promising Steep Slope Device Candidate?

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Abstract: Negative capacitance field effect transistors are another option for realizing steep switching transistors. Negative capacitance causes the differential potential drop in the semiconductor and the insulator to have opposite polarity, enabling MOS current to increase at a rate higher than 60 mV per decade. Recently, we have observed hysteretic switching with sub- kT/q steep slope (13 mV/decade at room temperature) in experimental devices by employing $\text{PbZr}_{0.52}\text{Ti}_{0.48}\text{O}_3$ (PZT) as a ferroelectric gate insulator, which was directly integrated on a silicon channel with a non-perovskite high- k dielectric (HfO_2) as a buffer interlayer. The sub- kT/q switching due to ferroelectric negative capacitance is observed not at low currents, but in strong inversion and provides an important point of consistency with predictions of Landau-Devonshire theory and Landau Khalatnikov equation. In this talk, we will review progress in non-perovskite ALD based ferroelectric dielectrics which have strong implication for VLSI compatible negative capacitance Ferroelectric FETs

Bio: Suman Datta recently joined the University of Notre Dame as the Chang Family Chair Professor of Engineering Innovation. He was previously a faculty member at Penn State University in Electrical Engineering. He joined Penn State as the inaugural Monkowski Associate Professor in 2007, and was promoted to Full Professor in 2011. Before joining Penn State, from 1999 till 2007, he was in the Advanced Transistor Group at Intel Corporation, where he developed several generations of logic transistor technologies including high- k /metal gate, Tri-gate and alternate channel CMOS transistor technologies. His research interests are in novel solid-state nanoelectronic materials and devices, understanding of transport mechanisms, and ultralow-power circuit applications, with recent emphasis on non-volatile computing powered by energy harvesters and computing using collective state of coupled systems. He was a recipient of the Intel Achievement Award (2003), the Intel Logic Technology Quality Award (2002), the Penn State Engineering Alumni Association (PSEAS) Outstanding Research Award (2012), the SEMI Award for North America (2012), IEEE Device Research Conference Best Paper Award (2010, 2011) and the PSEAS Premier Research Award (2015). He is a Fellow of IEEE.

