

NEEDS

Inter-band Tunnel Transistors: Opportunities and Challenges

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Abstract: Sustaining Moore's Law over the next decade will require not only continued scaling of the physical dimensions of transistors but also performance improvement and aggressive reduction in power consumption. Several device options beyond FinFETs such as GAA nanowire FETs are being pursued to extend technology scaling beyond 7nm node. Hetero-junction Tunnel FET (HTFET) have emerged as promising transistor candidates for supply voltage scaling down to sub-0.5V due to the possibility of sub- kT/q switching without compromising on-current (ION). Recently n-type III-V HTFET with reasonable on-current and sub- kT/q switching at supply voltage of 0.5V have been experimentally demonstrated. However, steep switching performance of III-V HTFET till date has been limited to range of drain current (IDS) spanning over less than a decade. In this talk, we will review progress in Tunnel FETs and also analyze primary roadblocks in the path towards achieving steep switching performance in III-V HTFET.

Bio: Suman Datta recently joined the University of Notre Dame as the Chang Family Chair Professor of Engineering Innovation. He was previously a faculty member at Penn State University in Electrical Engineering. He joined Penn State as the inaugural Monkowski Associate Professor in 2007, and was promoted to Full Professor in 2011. Before joining Penn State, from 1999 till 2007, he was in the Advanced Transistor Group at Intel Corporation, where he developed several generations of logic transistor technologies including high- k /metal gate, Tri-gate and alternate channel CMOS transistor technologies. His research interests are in novel solid-state nanoelectronic materials and devices, understanding of transport mechanisms, and ultralow-power circuit applications, with recent emphasis on non-volatile computing powered by energy harvesters and computing using collective state of coupled systems. He was a recipient of the Intel Achievement Award (2003), the Intel Logic Technology Quality Award (2002), the Penn State Engineering Alumni Association (PSEAS) Outstanding Research Award (2012), the SEMI Award for North America (2012), IEEE Device Research Conference Best Paper Award (2010, 2011) and the PSEAS Premier Research Award (2015). He is a Fellow of IEEE.

