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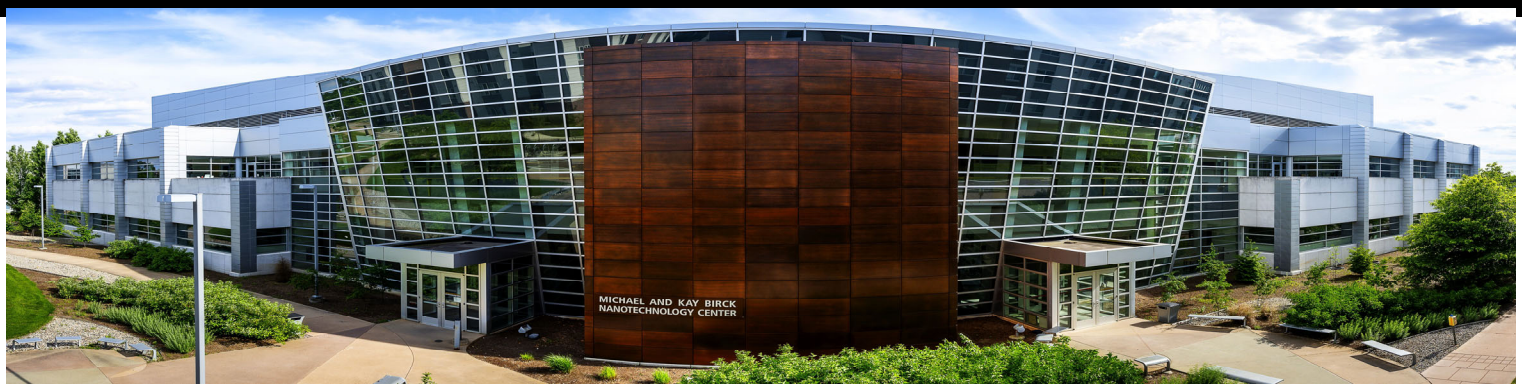

Atomic-layer-deposited atomically thin In2O3 transistors for BEOL logic and memory applications

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Date: Wednesday September 4th @ 2.00 pm in BRK 1001

Zoom Link: https://purdue-edu.zoom.us/j/95283400606

Bio: Dr. Peide Ye is Richard J. and Mary Jo Schwartz Professor at the School of Electrical and Computer Engineering, Purdue University. His research focuses on atomic layer deposition and its integration on various novel channel materials including III-V, Ge, 2D materials and complex oxides. He obtained his Ph.D. from Max-Planck Institute for Solid State Research in Germany and postdoc training at NTT Basic Research Laboratory, National High Magnetic Field Laboratory and Princeton University. He worked for Bell Labs of Lucent Technologies and Agere Systems before joining Purdue faculty in 2005. Prof. Ye received the 2011 IBM Faculty Award, Sigma Xi Award and Arden Bement Jr. Award. He is IEEE Fellow and APS Fellow for his contributions to materials and device development for compound semiconductor MOSFETs. Prof. Ye is also recognized as a Highly Cited Researcher among 6000 worldwide in all fields.

Abstract:
In this talk, we report on the first demonstration of atomically thin In_2O_3 channel for logic and memory devices by a back-end-of-line (BEOL) compatible atomic layer deposition (ALD) process [1]. High performance planar In_2O_3 transistors with high mobility of 153 $cm^2/V{\cdot}s$ and record high maximum drain current of near 20 mA/um are achieved by gate-all-around structure and thermal engineering [2]. ALD In_2O_3 3D Fin transistors are also demonstrated, benefiting from the conformal deposition capability of ALD. High-performance In_2O_3 ferro-electric transistors are demonstrated using ALD $HfZrO_2$ gating with >2.2V large memory window, >10 years retention and $>10^9$ endurance [3]. These results suggest ALD oxide semiconductors and devices have unique advantages and are promising toward BEOL-compatible monolithic 3D integration [4].

1. M. Si et al. IEEE EDL 42(2), 184-187, 2020; M. Si et al. Nano Lett. 21 (1), 500-506, 2020.

2. M. Si et al. VLSI, T2.4, 2021; Z. Lin et al., VLSI, 2024. Z. Zhang et al. IEEE EDL 43 (11), 1905, 2022; Z. Lin et al. ACS Nano 2022.

3. Z. Lin et al. IEDM, TF17.4, 386, 2021; Z. Lin et al. VLSI, TF13-2, 2022.

4. M. Si, Z. Lin et al. Nature Electronics 5(3), 164-170, 2022. A. Charnas et al., Advanced Materials, 2023.