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Central Indiana Chapter

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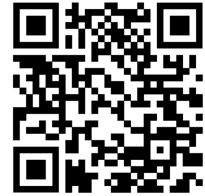
Why are Semiconductor Packaging & Heterogeneous Integration taking Center Stage for continuing Moore's Law?


(Scan here to register)

Dr. Madhavan Swaminathan

Time: Friday, April 5th, 2024, 1:00 PM – 2:00 PM (EDT)
Location: Online (via Zoom, joining link will be emailed to registrants)
Sponsors: IEEE Central Indiana EPS Chapter

Heterogeneous Integration (HI) provides the opportunity for dense connectivity between smaller dies from advanced technology nodes to improve yield, provides for connectivity between optimized legacy technology nodes to reduce time to market, and enables the connectivity of dissimilar dies on a single platform to enhance functionality. Though fueled by semiconductor packaging, HI represents higher levels of integration than what the semiconductor industry is used to and has done in the past. This is paramount to continuing Moore's law and making More than Moore possible.

As expected, this approach will pose many challenges but lots of opportunities as HI takes center stage. This presentation will cover the current state of the art, emerging applications, challenges that need to be addressed, and solutions being pursued.

Dr. Madhavan Swaminathan is the Department Head of Electrical Engineering and is the William E. Leonhard Endowed Chair at Penn State University. He also serves as the Director for the Center for Heterogeneous Integration of Micro Electronic Systems (CHIMES), an SRC JUMP 2.0 Center.

Prior to joining Penn State, he was the John Pippin Chair in Microsystems Packaging & Electromagnetics in the School of Electrical and Computer Engineering (ECE), Professor in ECE with a joint appointment in the School of Materials Science and Engineering (MSE), and Director of the 3D Systems Packaging Research Center (PRC), Georgia Tech (GT). Prior to GT, he was with IBM working on packaging for supercomputers.

He is the author of 650+ refereed technical publications and holds 31 patents. He is the primary author and co-editor of 3 books and 5 book chapters, founder and co-founder of two start-up companies, and founder of the IEEE Conference on Electrical Design of Advanced Packaging and Systems (EDAPS), a premier conference sponsored by the IEEE Electronics Packaging Society (EPS). He is a Fellow of IEEE, Fellow of the National Academy of Inventors (NAI), Fellow of Asia-Pacific Artificial Intelligence Association (AAIA), and has served as the Distinguished Lecturer for the IEEE Electromagnetic Compatibility (EMC) society. He has been recognized through many awards with the most recent one being the 2024 IEEE Rao R. Tummala Electronics Packaging Award (technical field award) for contributions to semiconductor packaging and system integration technologies that improve the performance, efficiency, and capabilities of electronic systems.

He received his MS and PhD degrees in Electrical Engineering from Syracuse University in 1989 and 1991, respectively.

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