EUV Lithography: History, Current Status, Technology Roadmap
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MSEE 190, Rice Design Studio

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Semiconductors@Purdue Distinguished Lecture
In partnership with IEEE Purdue Chapter and Purdue Semiconductor Student Alliance (SSA)

Talk Abstract:

Photolithography for semiconductor fabrication was invented in the 1950s. Until the early 1970s, contact and later proximity printing were the only lithographic methods used in semiconductor manufacturing. Projection lithography in high-volume manufacturing (HVM) began in the 1970s with the advent of Perkin-Elmer's unit-magnification wafer scanners and was advanced with the arrival of Hg g-line (436 nm) wafer steppers from GCA and others. Projection lithography's resolution capability is governed by the equation $\mathrm{HP_{min}} = k_1\,\lambda/\mathrm{NA}$ where $\mathrm{HP_{min}}$ is the minimum printable half-pitch (of a grating), NA is the numerical aperture of the imaging optics, and k_1 is a numerical factor with an absolute minimum value of 0.25. At that time, the "foreseeable" resolution limit of optical projection lithography was no better than 0.5 µm. Wavelength reduction below the Hg i-line (365 nm) was thought to be difficult to implement and high-NA lenses was considered difficult to fabricate without introducing a lot of aberrations. Various research groups started to work on so-called next-generation-lithography (NGL) technologies. Among the NGL technologies being pursued, extreme ultraviolet lithography (EUVL) was actually a late comer, with its long development process starting only in the mid-1980s. Meanwhile, optical lithography continued to make progress, culminating in $\lambda = 193\ \mathrm{nm}$ immersion lithography with an $\mathrm{NA} = 1.35$ and $k_1 < 0.3$ in routine production! Advances in optical lithography carried the geometrical scaling and provided the needed extra years for EUVL to mature.

EUVL finally entered the VHM of semiconductor chips in 2019, at the 7-nm node of logic integrated circuits, and enabled continued geometrical scaling. Since then, it has been used in research and development as well as the production of advanced logic and DRAM chips, and the performance of EUV exposure systems in imaging, overlay, and productivity

continues to improve. Meanwhile, after about ten years of development, 0.55 NA exposure systems became available in 2024. The latest lithographic results from such a system will be presented. High-NA EUVL will enable further scaling of logic and DRAM devices, and perhaps new-type devices of the future. So what's next? Like optical lithography, the resolution of EUVL also follows $\mathrm{HP}_{\mathrm{min}} = k_1\,\lambda/\mathrm{NA}$. Compared to optical lithography, the k_1 number for the current EUVL process is about 0.4. How to lower the k_1-factor further? Will there be exposure tools with an even higher NA? The presentation will conclude with a discussion on resolution enhancement and ASML's EUV technology roadmap.

Biography:

Anthony (Tony) Yen is VP and Head of the Technology Development Center at ASML, leading a global organization to work on identifying mid- and long-term technological directions in semiconductors and on accompanying patterning solutions in close collaboration with other organizations within ASML, imec, and universities. Tony received his BSEE degree from Purdue and his SM, EE, PhD, and MBA degrees from MIT. From 1991 to 1997, he was a Member of the Technical Staff at Texas Instruments. From 1997 to 2003 and again from 2006 to 2017, he was with TSMC where he led the development of its lithography processes and the development of EUV lithography for high-volume manufacturing. Tony is a recipient of the Outstanding Electrical and Computer Engineer Award from Purdue's ECE School. He is a Fellow of the IEEE and the 2026 recipient of its Cledo Brunetti Award, and a Fellow of SPIE and the 2023 recipient of its Frits Zernike Award for Microlithography.