PURDUE UNIVERSITY

Birck Nanotechnology Center

Material Driven Device Research for Post-Moore Era

Dr. Raisul Islam

Date: Tuesday March 26 @ 3:30pm in BRK 1001
(Coffee & Snacks @ 3.15pm)

Zoom Link: https://purdue-edu.zoom.us/j/99524580757

Abstract: By 2025, the global data creation is projected to grow to more than 175 zettabytes, where most of this enormous volume of the data will be unstructured and generated at the edge nodes. At the same time, the increasing size of machine learning training algorithms is causing increasing energy demand for computing. Therefore, the demand for chips capable of energy efficient high-throughput computation is limited by the Von-Neumann bottleneck, where the computational throughput and energy efficiency of the computation is limited by the data movement to and from the off-chip memory to the processing element. Current integration mechanisms for reducing the distance between memories and compute fabrics include the use of 2.5-D interposer or 3-D integration using wafer bonding and through silicon vias (TSV). Such methods cannot scale for too long since the aspect ratio of such structures and the mechanical stress limit aggressive scaling. In order to improve the computational throughput and energy efficiency by order of magnitude to handle the exponential growth of data, fine-grained and dense connectivity between memory and logic is required. In this scenario, monolithically 3D integrated system having multiple layers of transistors and memory stacked vertically connected by short high-density interlayer vias can be the ultimate solution. Such a system stands on technological breakthroughs that require fundamental materials innovation.

Therefore, the new era of abundant-data computation is heavily reliant on the fundamental advancements in the use of new materials in back-end CMOS processes to enable monolithically integrated 3-D chips with coexisting memory and logic. In this seminar, I will talk about some of my previous research projects on different emerging memory technologies that aim to enhance performance through new functional materials. First, I will demonstrate how a thermal barrier improves analog memory performance of resistive RAM (RRAM) known for its abrupt switching. Next, I will discuss different techniques to improve the energy efficiency of switching in phase change memory which is a significant bottleneck for its adoption in large scale on-chip memory array. Finally, I will discuss the path towards my vision for future research in realizing monolithically 3D integrated chip technology as a reality.

Bio: Dr. Raisul Islam joined MSE@Purdue as a tenure-track Assistant Professor in Spring 2024. His prior research focused on novel semiconductor devices, with expertise in thin-film deposition, device fabrication, characterization, and physics-based simulations of device performance. At Purdue, Raisul will lead a research group focusing on functionalization of new materials to realize monolithically integrated 3D systems for a range of emerging applications with a special interest in intelligent computation. Just prior to joining Purdue, Dr. Islam learned about 3D printing of battery as the Principal Scientist in Sakuu Corp., a series-B funded start-up in Silicon Valley that aims to revolutionize battery manufacturing. Previously, he also worked as a device technologist at SunRise Memory Corporation, a series-C funded new memory technology start-up also located in Silicon Valley that aims to revolutionize high speed highly scalable memory technology addressing some of the scaling challenges of DRAM. Prior to this, he worked at EMD Electronics, a leading material supplier to the semiconductor foundries, where he worked on the development of high temperature ALD precursors for ultra-thin ferroelectric films at low thermal budget. Raisul has also briefly worked at Taiwan Semiconductor Manufacturing Company (TSMC) in the corporate research division. Before joining industry, Dr. Islam completed his PhD in Electrical Engineering from Stanford University in 2017 under the supervision of Professor Krishna Saraswat. He then worked as a post-doctoral scholar with Professor H.-S. Phillip Wong from 2017 – 2019. His PhD work on ultra-thin photovoltaics has resulted in seed grant award from TomKat Center for Sustainable Energy at Stanford. He was also the recipient of Eric and Illeana Benhamou Stanford Graduate Fellowship. Raisul Islam obtained his B.Sc. and M.Sc. degrees in Electrical and Electronic Engineering from Bangladesh University in Engineering and Technology in 2009 and 2011 respectively. He was a recipient of University Gold Medal for graduating summa cum laude in 2009. He is an author of numerous scientific publications and inventor in numerous patent applications.

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