IEEE ELECTRONICS PACKAGING SOCIETY
Central Indiana Chapter

PURDUE UNIVERSITY

Co-Packaged Optics- Heterogeneous Integration of Photonic IC and Electronic IC

Dr. John H Lau

Time: Tuesday, March 5th, 2024, 12:00 PM – 1:00 PM (EST)
(The food will be served 15 mins prior to noon)
Location: BRK 1001 (Birck Nanotechnology Center)
1205 W State St, West Lafayette, Indiana 47907
Sponsors: IEEE Central Indiana EPS Chapter

Silicon photonics are the semiconductor integration of EIC and PIC on a silicon substrate (wafer) with complementary metal-oxide semiconductor (CMOS) technology. On the other hand, co-packaged optics (CPO) are heterogeneous integration packaging methods to integrate the optical engine (OE) which consists of photonic ICs (PIC) and the electrical engine (EE) which consists of the electronic ICs (EIC) as well as the switch ASIC (application specific IC). The advantages of CPO are: (a) to reduce the length of the electrical interface between the OE/EE (or PIC/EIC) and the ASIC, (b) to reduce the energy required to drive the signal, and (c) to cut the latency which leads to better electrical performance. In the next few years, we will see more implementations of a higher level of heterogeneous integration of PIC and EIC, whether it is for performance, form factor, power consumption or cost. The content of this lecture is shown below.

Silicon Photonics
Data Centers
Optical Transceivers
Optical Engine (OE) and Electrical Engine (EE)
OBO (on-board optics)
NPO (near-board optics)
CPO (co-packaged optics)
Integration of the PIC and EIC
2D Heterogeneous Integration of PIC and EIC
2D Heterogeneous Integration of ASIC Switch, PIC and EIC
2D Heterogeneous Integration of ASIC Switch, PIC and EIC with Bridges
3D Heterogeneous Integration of PIC and EIC
3D Heterogeneous Integration of ASIC Switch, PIC and EIC
3D Heterogeneous Integration of ASIC Switch, PIC and EIC with Bridges
Heterogeneous Integration of ASIC Switch, PIC and EIC on Glass Substrate
Summary

(Scan here to register)

Dr. John H Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging, has published more than 530 peer-reviewed papers (385 are the principal investigator), 52 issued and pending US patents (31 are the principal inventor), and 23 textbooks (all are the first author). John is an elected IEEE fellow, IMAPS Fellow, and ASME Fellow and has been actively participating in industry/academy/society meetings/conferences to contribute, learn, and share.

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