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PURDUE UNIVERSITY Discovery Park

How to Write, Develop and Implement a *Real* Compact Model

A hands-on workshop by Dr. Colin McAndrew
Freescale Semiconductor

Conducted at Purdue University
1:30 PM Nov. 18 – noon Nov. 19, 2014
DLR 131

Abstract – Compact models must get the physics right, work reliably over bias, geometry, and temperature, interact properly with the circuit simulators in which they are implemented, run efficiently, and follow good software development practices. This workshop will be a detailed deep-dive into an industrial strength Verilog-A code for the R3 model for JFETs, diffused resistors, and polysilicon resistors. Do not think that a "resistor" is a trivially simple device to model: real resistors are affected by depletion pinching, velocity saturation, and self-heating, and to properly account for all of these effects, while ensuring no unphysical model behavior, is not trivial. But it is not as complex as a complete MOS or bipolar transistor model – so it is ideal as a training vehicle for compact modeling.

Who should attend – This workshop is designed for those who are new or still fairly new to compact modeling. Those who have never written a compact model should be prepared to write a "simulation-ready" compact model. Those who have limited experience should learn how to write better models. To benefit most from this workshop, participants should have an elementary acquaintance with the Verilog-A language and the R3 model, as gained from the pre-workshop reading assignment.

Instructor – Dr. Colin McAndrew has been involved in compact modeling of bipolar, MOS, and passive devices for more than 25 years. Dr. McAndrew is a Fellow of the Technical Staff at Freescale Semiconductor, Tempe, AZ.

For more information and to register: https://nanohub.org/groups/needs/verilogwkshp

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