PURDUE UNIVERSITY

Birck Nanotechnology Center

Advanced Manufacturing for Semiconductor Packaging and Electronic Cooling

Dr. Tiwei Wei

Assistant Professor, School of Mechanical Engineering

Date: Wednesday 4/17/2024 @ 3.00 pm in BRK 1001

Zoom Link: https://purdue-edu.zoom.us/j/91824104539

Abstract:

Advanced semiconductor packaging is playing a crucial role to drive system performance and functionality. With the increasing demand for emerging and growing computing needs, heterogeneous three-dimensional (3D) integration with fine-pitch, high-density interconnections, and multi-chip stacks are very promising in the future. The aggressive interconnects pitch scaling and nanoscale via interconnections make the process development and reliability more and more challenging. On the other hand, this high-density 3D integration system has resulted in a substantial increase in both heat flux and power density (W/cm^3). High-performance, energy-efficient thermal management solutions are needed to tackle this thermal challenge. During this talk, I will first present the copper 3D interconnects manufacturing technologies and their applications in different heterogeneous 3D integration systems. The second part of this talk will focus on the micro/nano fabrications and package integration of advanced on-chip thermal cooling solutions, including impingement jet cooling, and manifold-based embedded microchannel cooling.

Bio:

Dr. Tiwei Wei is an Assistant Professor at Purdue University's School of Mechanical Engineering. Prior to his role at Purdue, he completed a postdoctoral research tenure in Stanford University's NanoHeat lab between 2020 and 2022. He received his Ph.D. degree in the 3D system integration department at Interuniversity Microelectronics Centre (imec) and KU Leuven, Belgium in 2020, focusing on developing electronic cooling solutions for high-performance 3D systems. Before that, he held senior research positions at Tsinghua University and Hong Kong University of Science and Technology from 2011 to 2015, delving into advanced microelectronic packaging techniques. His current research emphasis encompasses advanced semiconductor packaging and heterogeneous integration, spanning processing, materials, architecture development, chip-package interactions, reliability, and efficient thermal management technologies. He authored over 60 scientific publications in leading journals, conference proceedings, and authored over 10 patents. Dr. Wei actively contributes to the academic community, serving as a session chair and member of the technical program committee in various electronic packaging conferences like IEEE ESTC, REPP, 3DIC, SHTC, Itherm and EPTC. Additionally, he has held leadership roles such as vice-chair of IEEE Electronic Packaging Society (EPS) Silicon Valley Chapter and currently the founder and chair of IEEE EPS Central Indiana Chapter.