Job Category: R&D

Primary Location: West Lafayette, IN and Berkeley, CA, USA

Job Title: Process Engineer

Job Description:

Kepler Computing is building fundamentally new blocks to accelerate computation beyond Moore's law. The founding team consists of industry veterans spanning across the full compute stack of product, architecture, circuit, device, manufacturing and physics.

Materials and process development are an integral part of Kepler Computing. In this highly visible role of a Process Engineer, you'll join a team helping to develop the most efficient means for device processing, enabling computing systems to do more with less energy. Process Engineers take responsibility for specifying and developing dry etch solutions for various thin film stacks or mono-layers, as well as assist with ongoing efforts to integrate new etch solutions into our integrated device process flows. You will take a demanding set of functions and turn them into the computing technology that transforms how the world works, plays, learns and communicates. If you are looking for a position where you can see the end results of your work making a real impact on the tech world and on real experiences, this is the position for you.

The candidate must execute projects based tasks that include process development, integration and metrology/characterization of materials working side-by-side with a diverse group of engineers to solve problems creatively with deadlines; assume ownership and accountability for successful completion of projects and programs; report results both internally and externally with presentation and formal report packages; interact with other engineers in areas of design, growth, fabrication and test to facilitate fabrication and device optimization; metrology and defectivity experience and process development established within coupon line, 100mm, 150mm and 300mm fabrication line.

This position will initially be situated in West Lafayette, IN for about the first 3 months. The candidate will need to perform R&D work at Purdue University’s Birck Nanotechnology Center. After the initial period as mentioned above, the candidate will need to relocate to Berkely, CA.

The candidate is expected to have good oral and written communication skills and experience in technical writing. Equipment that will be used during the course of performing essential functions include RIE and IBE etch tools, SEM, AFM and other analytical instrumentation and some physical tasks may require standing and walking, lifting objects up to 20 pounds, and the use of hand tools.

Roles and Responsibilities:

- Ownership of RIE and IBE etch development projects of various thin film mono-layers or stacks of both dielectric and metal films. On a daily basis support:
    - Etch recipe development and characterization
    - Etch tool baseline checks
    - Etch profile characterization using Scanning Electron Microscopy (SEM), Focussed Ion Beam microscopy (FIB), and Energy Dispersive X-Ray Analysis (EDX)
    - Film resistance metrology by 4-point probe
    - Film thickness measurements using ellipsometry
    - Other occasionally used techniques like Raman spectroscopy, Infrared spectroscopy, digital scanning calorimetry, Atomic Force Microscopy etc.
- Coordination of external metrology analysis
- Participate in running other process modules such lithography, and PVD deposition as required by team
- Statistical Data analysis including plotting graphs and curve-fitting using appropriate software tools
- Participate in working group meetings with group to review data and design new experiments
- Writing patents and publications
- Preparing and presenting scientific presentations to group and upper management, as well as to customers, investors and advisors
- Participate in equipment procurement activities and associated planning projects
- Participate in equipment installation and qualification projects

Minimum Requirements:

The candidate must possess a minimum of an M.S. in Materials Science, Chemical Engineering, Chemistry, Physics, Electrical Engineering or related subject.

Preferred Qualifications:

- PhD will be preferred
- Substantial experience in dry etching using RIE, especially etching patterns on mono-layers or stacks. Knowledge of Ion Beam Etching a plus
- In-depth knowledge of various RIE plasma mechanisms, instrumentation is highly desirable
- Experience in Data analysis (one or multiple of data analysis tools, JMP, SPC, Origin, MATLAB, Mathematica, MS Office), Design of experiment (DOE) principles, industry standard semiconductor processes
- Be able to apply the fundamentals of materials science and engineering.
- Prior experience in various measurement techniques such as XRD, XRR , AFM , RBS, PFM , XRF , EDX , TEM, SEM , Ellipsometry, XPS etc.
- A good understanding of FEOL and BEOL semiconductor integration schemes, in addition to knowledge and experience in logic and memory device fabrication
- Good program management and customer interface skills are essential. The successful applicant must be able to interface effectively with fab operations, process maintenance, and semiconductor engineering professionals from client companies.

Posting Statement

All qualified applicants will receive consideration for employment without regard to race, color, religion, religious creed, sex, national origin, ancestry, age, physical or mental disability, medical condition, genetic information, military and veteran status, marital status, pregnancy, gender, gender expression, gender identity, sexual orientation, or any other characteristic protected by local law, regulation, or ordinance.

Compensation is highly competitive by industry standards.

Please email your resumes or questions to debraj@keplercompute.com.